Crack Catcher AI – Enabling Smart Fracture Mechanics Approach for Damage Control in Thin Silicon Wafers for 3D Semiconductor Integrated Devices/Packages

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***Abstract*— The importance of silicon cannot be undermined – in photovoltaics (PV) as well as in semiconductor industries. However, silicon is very brittle. Silicon cells/wafers crack easily during manufacturing assembly and/or during device operations. *Crack Catcher AI* uses novel smart fracture mechanics approach with Artificial Intelligence (AI) methodologies to predict and control crack/damage evolution in thin silicon cells/wafers. This is critical as semiconductor 3D integration technology calls for wafer-to-wafer bonding with utmost alignment accuracy and yield/reliability.**

***Index Terms*-- 3D Integrated Devices/Packages, Fracture Mechanics, Machine Learning Approaches, Silicon Crack**

I. INTRODUCTION

Silicon is a crucial material in modern technology, particularly in its thin-layer geometry, including in semiconductor industry. Most recently, thin silicon wafers (less than 1 mm thickness) with large diameters (up to 300 mm or 12 inches) even need to be bonded wafer-to-wafer to enable 3D integration of microelectronics devices/packages. One of the key issues in Wafer-to-wafer bonding process is making sure the chips are all aligned within the specific target of Ultimate Bond Pad Pitch Target < 1 μm, with Pad to Pad Placement Accuracy (x, y) Target <10% of bonding pitch, for silicon semiconductor wafers as large as 300 mm and chiplet sizes as small as 2 x 2 mm [1].

Semiconductor wafers go through various thermal and mechanical processes during their Front-End and Back-End manufacturing sequence in the wafer fab. As a result, mechanical stress resides in the wafers, and especially in large wafers (300 mm diameter). The semiconductor industry has recognized this general issue and has used wafer curvature measurement techniques so far to manage stress due to thermomechanical processes as well as the introduction of new thin film materials in the past 10-15 years or so. However, this wafer curvature technique is mostly effective for determining the global stress in the wafers. Wafer-to-wafer bonding requires highly precise alignment between chips on one wafer to the chips on the other wafer it is to be bonded on, as illustrated in Fig. 1. Global or overall mechanical stresses in large semiconductor wafers have already made this quite challenging, but whether all chips in the large wafer can be aligned within the specific targets depends also on the local stresses which vary from location to location in the wafers. Even very small strains, such as exemplified in Fig. 1, could lead to large misalignment in the wafer-to-wafer bonding. Furthermore, these local stresses can lead to surface microcracks on wafers (either top or bottom) and result in even larger misalignments.

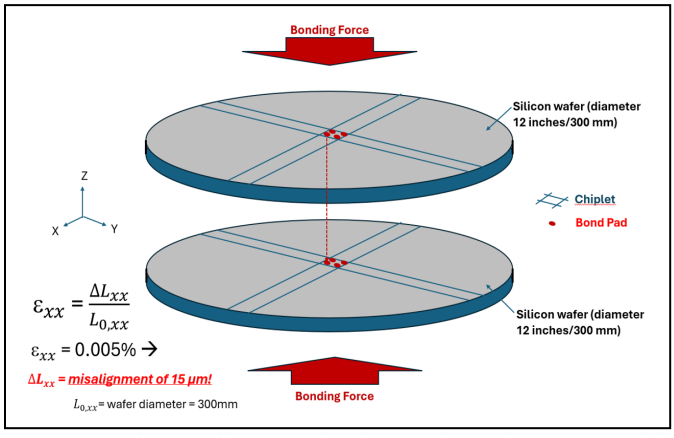

Figure 1. Schematic illustration of Wafer-to-wafer bonding process and the key issue of misalignment due to local stresses in the large, thin silicon semiconductor wafers.

Our proposed solution is ***Crack Catcher AI*** – Smart Fracture Mechanics Approach in Thin Silicon Semiconductor Wafers for Enabling Wafer-to-wafer bonding in 3D Semiconductor Integrated Devices/Packages. It is about a local stress metrology tool that would allow rapid mapping of local stresses in a silicon semiconductor wafer which enables use in high volume manufacturing or packaging assembly environments. With the local stress map in each wafer, each potential misalignment on every chip on the wafer may be mapped and optimization of alignment process of each wafer in the Wafer-to-wafer bonding process both in X and Y directions may be done in fast, quantitative and with high confidence for the best results for manufacturing or packaging assembly yield. Our proposed technique for the local stress metrology is not based on the typical X-Ray Diffraction (XRD) or Raman methodology – in which case, rapid mapping of local stress has not been possible or practical. Our technique in the ***Crack Catcher AI*** method uses a laser system to detect local surface misorientations across the silicon wafer and correlate those to local stresses. Hence, the rapid mapping ability of the local stresses in a silicon semiconductor wafer.

Our collaborative team has developed the ***Crack Catcher AI*** methodology mostly for determining local stresses in the silicon solar cells which have led to propagation of cracks in the solar cells – one of the top 3, if not top 2, reliability issues in the industry. Cracks occur in the silicon cells even when they are already integrated within the solar panels and in operation in the fields. They propagate due to mechanical stress or loads from winds, snows or storms which happen in ordinary circumstances in the fields, especially in four-season countries, like the U.S.A. Over time, when these cracks propagate to many of the areas in a solar cell, power production from that cell degrades significantly, and eventually affects the performance of the overall solar panel. Hence, these cracks are defects that can compromise the efficiency (power production) and longevity (lifetime) of photovoltaic (PV) modules.

The ***Crack Catcher AI*** was our research joint collaboration's entry in the Department of Energy (DOE)'s American-Made Solar Innovation competition in 2022 (Round 6) which later was selected as the national semifinalists and won an award announced by DOE in December 2022 [2]. This system employs smart stress sensing and smart fracture prediction methods, integrating fundamental fracture mechanics with big data analytics to minimize cracks and enhance the durability of PV products. Smart Stress Sensing utilizes a laser-based curvature technique for rapid in-line stress measurement, while Smart Fracture Prediction applies AI for defect detection and yield improvement in PV production. While our study thus far has been primarily focused on monocrystalline silicon solar cells (for the applications of reliability improvement in the silicon solar PV industry), the principles and innovations discussed are also applicable to single crystal silicon semiconductor wafers. The present manuscript represents our efforts to apply the ***Crack Catcher AI*** methodology for enabling Wafer-to-wafer bonding process in the semiconductor industry. Much of the findings reported here are therefore mostly from the silicon solar cells, but we include our analysis on how they could enable chip alignment accuracy in the wafer-to-wafer bonding scheme, as well as enhancing semiconductor manufacturing yield (by damage/defect control of semiconductor wafers) along with improving semiconductor product quality and reliability.

II. METHODOLOGIES

Silicon, especially in its most useful thin layer form, is inherently brittle and prone to cracking during the manufacturing of solar cells or semiconductor wafers. In the PV industry, these cracks are defects that can compromise the efficiency and longevity of PV modules. Silicon solar cells are becoming increasingly thinner as technology advances. One drawback of this trend is higher stress concentration during the manufacturing processes. This is resulting in deteriorating efficiencies and long-term reliability of the silicon solar cells. The ***Crack Catcher AI*** is using high-resolution laser techniques to achieve similar quantitative stress that is built on previous work using synchrotron X-ray microdiffraction [3,4], to map stress in silicon cells. A smart stress sensing tool for inline production, improving fracture prediction and manufacturing yield is in development by leveraging AI and data analytics. The present manuscript outlines two key systems: Smart Stress Sensing (using laser technology) and Smart Fracture Sensing and Prediction (utilizing AI), both aimed at enhancing the efficiency and cost-effectiveness of next-generation solar silicon PV technologies (as shown in Fig. 2).

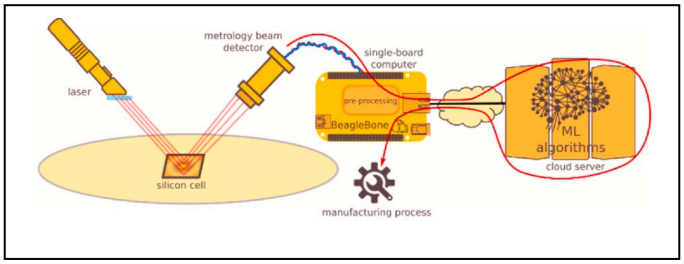

Figure 2. Schematic illustration of optical (laser-based) inline metrology system and the data processing via BeagleBone and big data analysis by cloud computing machine algorithms. Reproduced with permission from Elsevier B.V [2].

The Smart Stress Sensing (SSS) System is based on high-resolution laser instrumentation and enabled by the local curvature technique (Stoney's equation) [3,4]. This technique is used to measure the local stress and map it as a function of position (X, Y) across the large silicon semiconductor wafer in high resolution (micron-scale), such as illustrated in Fig. 2. The principle of measuring local stress in a thin silicon plate form based on local curvature has been successfully demonstrated [2,5-7] on silicon solar cells, such as shown in Fig. 3. Moreover, stress determination based on local curvature (Stoney's equation) has been correlated with the stress determination based on synchrotron X-ray microdiffraction [5,6]. These are two different physics in measuring local stress in thin plate forms, and yet the results are correlated very well [6]. The mapping of local stress in a silicon semiconductor wafer using the local curvature method has not been demonstrated so far, but the scientific principles apply (both silicon solar cells and semiconductor wafers are on thin plate forms – where the Stoney's equation would apply, only different in thicknesses, solar cells are about 200 μm and semiconductor wafers are about 500-800 μm, and both

are made out of single crystal silicon materials with the laser essentially reflecting on the same surface). It is within the scope of this proposal to demonstrate the basic feasibility of the **SSS** system for silicon semiconductor wafers.

The Smart Fracture Sensing & Prediction (SFSP) System is based on AI (Artificial Intelligence) and big data analytics. This technique is used to detect and image defect/crack, map it as a function of position (X,Y) across the large silicon semiconductor wafer in high resolution (micron-scale) and predict the damage evolution or crack propagation based on AI and Machine Learning approaches, such as illustrated in Fig. 2. The basic principle of mapping and predicting the crack propagation has been successfully demonstrated [2] again on silicon solar cells. It is not yet done on silicon semiconductor wafers but again for similar reasons mentioned above (both are silicon single crystals on thin plate forms), the crack pattern prediction will be practically the same. On reference [2], we have demonstrated the ability of our **SFSP** system to predict the major directions (+/- 45°) of crack propagation in the single crystal silicon solar cells, as shown in Fig. 4. However, since then, we have also extended our work on the **SFSP** system to include the classification, clustering, correlating and predicting the other crack propagation lines (minor crack propagation pattern) observed in silicon solar cells from various manufacturers occurring due to ordinary circumstances (default operational conditions in the fields like wind, snow or storm, not extraordinary circumstances like fires, hurricanes or typhoons). Our **SFSP** system has been successful in classifying, clustering and correlating them, which are the mandatory initial steps for eventually predicting them. We present our most recent findings with the **SFSP** system in the Section: SPSF's Ongoing Algorithm Development for Crack Prediction Beyond the Major Directions (+/- 45°) later in the present manuscript. This work will be continued and extended to typical surface crack propagation patterns observed in the silicon semiconductor wafers in this proposed work.

In similar veins, many of our technical discussions in later sections of the present manuscript will be primarily based on our recent results with monocrystalline silicon solar cells, but they form the basis for our main argument in this proposal – that the **SSS** and the **SFSP** systems' abilities will be applicable for silicon semiconductor wafers, and when done on manufacturing/packaging floors, they can help enhance misalignment precision and process in wafer-to-wafer bonding scheme for the semiconductor packaging industry, and will improve semiconductor manufacturing/packaging yield and device/product lifetime and reliability assessment.

III. DATA/RESULTS

A. *Smart Stress Sensing (SSS)*

Silicon solar cells are becoming increasingly thinner as c-Si (crystalline silicon) solar photovoltaics (PV) technology advances. One drawback of this trend is higher stress concentration during the manufacturing processes. This is resulting in deteriorating efficiencies and long-term reliability of the silicon solar cells. This study is using high-resolution laser techniques to achieve similar quantitative stress that is built on previous work using synchrotron X-ray microdiffraction [7,8], to map stress in silicon cells. A smart stress sensing tool for inline production, improving fracture prediction and manufacturing yield is in development by leveraging AI and data analytics.

Previous research using synchrotron X-ray microdiffraction (μSXRD) effectively mapped stress and crack propensity in silicon solar cell assemblies, allowing for precise stress quantification in high-stress areas. The current study aims to use a new stress sensing technique that replaces synchrotron radiation with a high-resolution laser source, while maintaining similar quantitative capabilities. This innovative approach aims to provide a detailed examination of stress and its evolution during real-world operational processes of solar devices [2]. The **SSS** technique aims to extend existing wafer curvature measurement methodologies to enable localized stress assessments in solar cells, using a lab-based system with higher resolution specifications [2,3,9] This approach allows for real-time stress measurements during manufacturing, facilitating faster innovation in cell design and architecture, particularly for ever larger silicon wafers and advanced 3D integration package designs.

Our latest **SSS** results are shown in Fig. 3, using the laser set up (not the synchrotron set up). Fig. 3(a) shows the experimental stress maps obtained from the laser measurement on areas around a metallization interconnect on the monocrystalline silicon cells. They show the high local stress concentration areas on the edges of the metal lines. Fig. 3(b) shows the simulation using FEA indicating good agreement to the experimental stress maps.

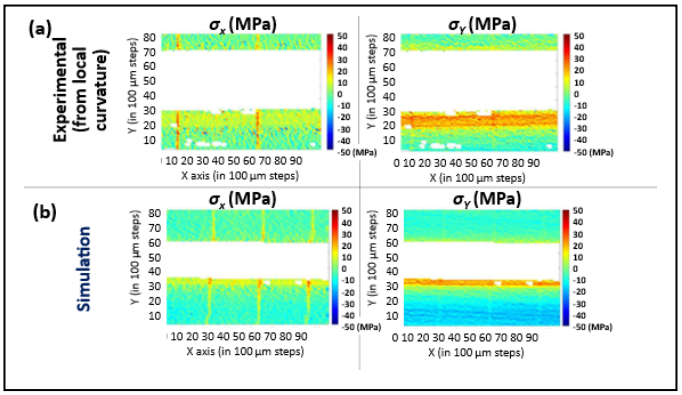

Figure 3. Comparison between (a) Experimental and (b) Simulation results in the monocrystalline silicon solar cell (unlaminated). The comparison suggests high degree of consistency in showing the high stress concentration areas (the stresses in X-direction (sx) and Y-direction (sy)) [2]. Reproduced with permission from Elsevier B.V [2].

B. *Smart Fracture Sensing & Prediction (SFSP)*

The development of SFSP system is designed for real-time data collection and analysis in high-volume c-Si photovoltaic manufacturing. The system integrates an inline curvature measurement tool that transmits processed data to a cloud infrastructure for advanced statistical analysis using artificial intelligence (AI), as shown in Fig. 2 [2]. This data can be used to create crack/defect maps of the cells, facilitating predictions of crack initiation and propagation through a combination of Finite Element Analysis (FEA) and AI algorithms.

The results of the **SFSP** experiments for predicting PV crack using the Long Short-Term Memory (LSTM) algorithm as a Time Series Regression Predictor are demonstrated in Fig. 4 below [2]. The image shows the crack's prediction results, which can be tracked into sequences of time. We compare our results with the actual condition of the PV crack picture, which is generated using a specific instrument developed in the laboratory to obtain a sequenced cracked PV over time. The results suggest that prediction can be made properly for a linear crack event in major directions (+/- 45° angles). The angle definition here uses the convention in solid mechanics [21] – in the Cartesian coordinate system, the +X direction is 0° and then the angle goes positive counter-clockwise (CCW), hence the +Y direction is +90°, the -X is 180° and the -Y is 270°.

While results as shown in Fig. 4 have successfully predicted the major directions of crack propagation (+/- 45° angles), the complete crack propagation patterns as shown in Fig. 5 remain elusive [10-12]. In addition to the major directions (+/- 45° angles), cracks tend to branch to other random directions (not necessarily following crystallographic planes or directions) [12-19]. Our ongoing work on the **SFSP** system which will be discussed in the following section aims to train our algorithm based on large data sets of cell crack patterns and enable crack prediction, and hence damage control for enhancing manufacturing yield and product reliability. The Reinforcement Learning (RL) algorithm is infused with the physics associated with fracture mechanics and the material science/crystallography of the monocrystalline silicon cells.

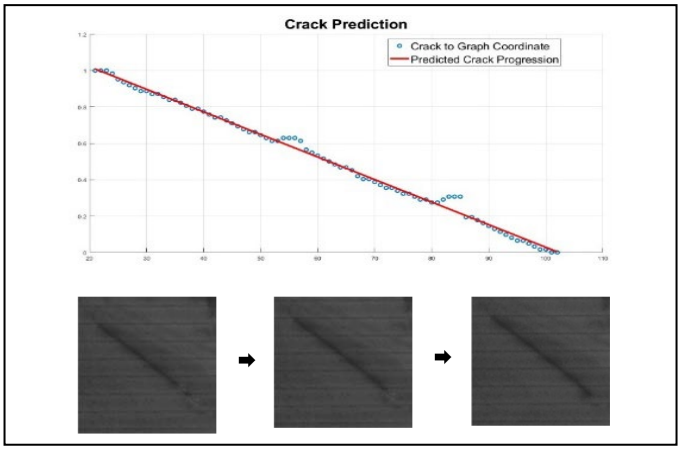

Figure 4. The Crack Prediction result shows the capabilities to predict the future event of a crack in a silicon solar cell in the major directions (+/- 45° angles) compared to the actual condition (below) of a crack propagation in the cell [2]. Reproduced with permission from Elsevier B.V [2].

C. *SPSF's Ongoing Algorithm Development for Crack Prediction Beyond the Major Directions (+/- 45°)*

In this work, we have conducted a preliminary extension by capturing repeated angle of cracks which are happening not totally in random but following crystallographic planes in this case for monocrystalline silicon PV cells. These repeated patterns are captured by two approaches, firstly by image processing (computer vision) approach supported by heuristics / hand-crafted rules (classical AI) for preprocessing and classification task (Fig. 6). The rules implemented are the variation in angle of cracks according to first principles physics (crystallographic planes). The experiment was conducted on public dataset of PV crack cells [20]. The experiment results are shown in Figure 7. In these figures, the heuristic-based algorithm has marked all different crack lines and classify them by showing in different colour mark as different angle. The major angle are the ones shown in green which are the +/-45°. The other are different angles shown in blue and in orange which are happening in different frequencies (less frequent than the +/-45°).

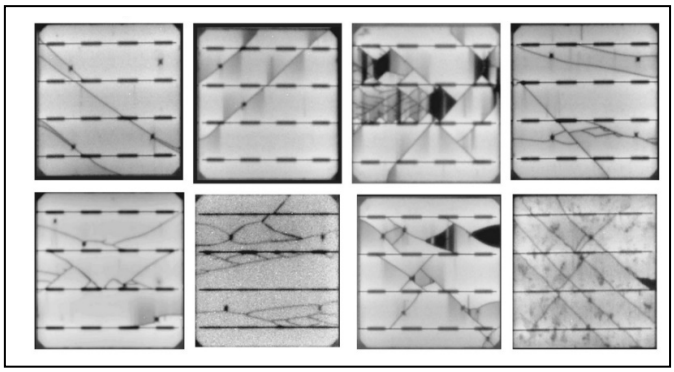

Figure 5. Typical complex crack patterns in monocrystalline silicon solar cells – major directions (+/- 45° angles) with branches in multiple random directions [10-12]. **Reproduced with permission from Elsevier B.V [2]**

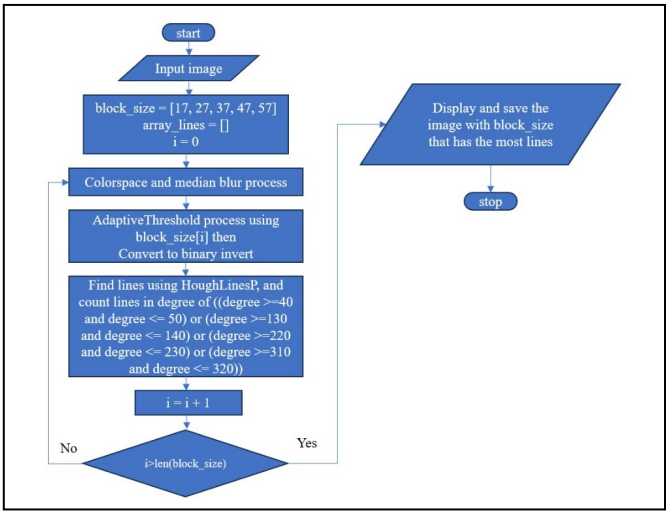

Figure 6. Heuristic-based (Classic AI) approach for detecting crack

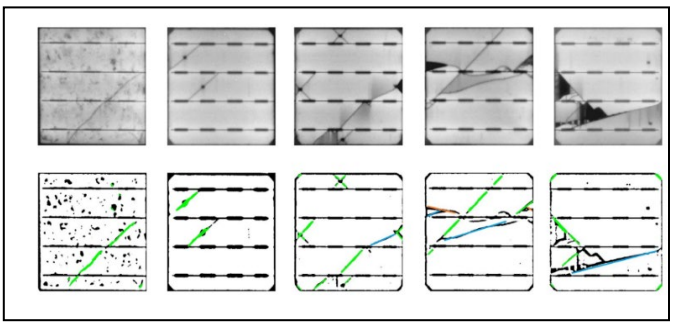

Figure 7. Heuristic (Classic AI) experimental results.

In the second approach we have conducted a combination of object (crack) detection and classification task by machine learning approach utilizing deep learning architectures [22-25] for learning different kinds of crack patterns (angle) also based on the same public dataset of PV crack cells [20]. It follows machine learning methodology of training, validating and testing procedure to be able to generate the logic for detecting and classifying crack patterns which we have confirmed as in sync with results from first principles patterns. We use computer vision-based preprocessing utilizing OpenCV [26] framework which include filtering and thresholding and applying convex hull algorithm for identifying cell areas, this forms an image processing pipeline according to methodology provided in pvimage Phyton package [24,25]. As a following procedure to perform object (crack) detection, we use Yolo deep learning framework which is an extension of Convolutional Neural Network (CNN) architecture [27] and to perform classification we use Residual Network (Resnet) architecture (also on improved version of CNN) [28] according to methodology provided in pv-vision [22,23]. Both architectures are trained, validated and tested using the public dataset provided by the Duramat Consortium [20]. The preliminary results of these experiments are shown in Table 1 (with accuracy among the detected lines = 98.6%). This result indicates that 75.4% of all the crack lines belong to the angles (+/- 45°, +/- 6° and +/- 13°) that may be correlated with certain crystallographic planes of the single crystal silicon of the solar cell. This implies that crack propagates along certain preferred crystallographic planes at least 75.4% of the time, which has an important role in crack prediction. Whether the remaining 24.6% of time may be further predicted by deep learning methodology or they are completely random (statistically) in a time series model [29] remains our continued study for the **SPSF** system development.

Angles Detected	Frequency / Count	Total Frequency Detected	Total Frequency	Occurrence (Detected) (%)	Overall Occurrence (%)
+/- 45°	166	278	310	59.7	53.5
+/- 6°	35	278	310	12.6	11.3
+/- 13°	33	278	310	11.9	10.6
+/- 20°	14	278	310	5.0	4.5
+/- 40°	8	278	310	2.9	2.6
+ 60°	8	278	310	2.9	2.6
+ 120°	7	278	310	2.5	2.3
+ 90	3	278	310	1.1	1.0
+ 110°	3	278	310	1.1	1.0
+ 70°	1	278	310	0.4	0.3
Undetected	32	NA	310	NA	10.3

TABLE I. CRACK LINES DETECTION RESULTS USING OBJECT DETECTION BASED ON YOLO V3 AND RESNET 18 – REORDERED BY RANK

IV. DISCUSSION

The findings thus far as reported in the present manuscript have been primarily on silicon solar cells for the purpose of manufacturing yield enhancement as well as product reliability/quality improvement along with product warranty management which are of utmost importance for the solar PV industry. The ***Crack Catcher AI*** system (consisting of the two key components – the Smart Stress Sensing/SSS and the Smart Fracture Sensing & Prediction/SFSP systems, as shown in Fig. 2, could be further developed to be implemented as a pilot-line metrology tool that will be used in high-volume packaging assembly environments in semiconductor industry (specifically which involves wafer-to-wafer bonding in the 3D integration of packages/devices).

The **SSS** system could provide mapping capability of local stress in large silicon semiconductor wafers (300 mm) to determine adjustments needed to make sure super-critical alignment precision in the wafer-wafer bonding – the **SSS** system. As shown in Fig. 1, a mere strain of 0.005% in the silicon (certainly has been observed in typical semiconductor wafers even during back-end interconnect [30,31] or Through-Silicon Via (TSV) [32,33] processing) could lead to several microns of potential chip-to-chip misalignments, which will have detrimental effects on the chip performance. While the fundamental issue is stress, its existence in the silicon wafers in the semiconductor industry is inevitable due to the many thermomechanical recursions that the wafers must endure during the creation of the integrated circuits and their interconnection networks. This situation is of course further aggravated by the current trend of 3D integration with TSV for instance which makes the stress states in the silicon semiconductor wafers become even more complicated and 3D in nature (instead of just primarily 2D stress states in the older planar semiconductor technology generations). With the Wafer-to-wafer bonding, the stress maps provided by the **SSS** system would make the optimization of the alignment process between two wafers more quantified and thus could be done more systematically, faster and thus more effectively.

The SFSP system could provide the map of defect/crack and predict crack propagation in large wafers to allow quantitative prediction to be made to enhance manufacturing yield and device reliability. The silicon wafers in the semiconductor industry are typically much thicker (usually 500-800 microns) compared to the silicon solar cells (typically 150-250 microns), and that is the reason why through-thickness cracks were less observed in the semiconductor industry. Having said that, many surface cracks and damages (dents, scratches, etc.) were observed in semiconductor wafers and they might lead to issues ranging from manufacturing yield loss, assembly/packaging issues down the line to eventually product quality and reliability [34]. While the SFSP in the silicon solar cells has been used mostly for predicting crack propagation on the plane of the cells, its principles could be further extended to prevent propagation of the surface cracks in the semiconductor wafers through the thickness of the silicon wafers. The fracture mechanics and the silicon crystallography will be exactly the same. The AI code, especially when it comes to the rapid learning of how crack propagates in silicon single crystalline structure may be re-used with minor modifications. In fact, it is more critical for the surface cracks in the semiconductor wafers, and hence the impact will be greater. Surface cracks in the silicon semiconductor wafers only have say 800 microns of the total thickness of the wafers – the much higher ratio between the crack size and the overall dimension of the product (in this case, the thickness of the wafers) creates much higher driving force for the crack to propagate through the thickness, which could lead easily to chip performance issues, if not its complete breakdown.

V. CONCLUSIONS

The ***Crack Catcher AI*** (***CCAI***) is a system that uses two key components. The first is a smart sensing technique that uses high resolution laser measurements to create a stress map of the silicon cell. The second component is an AI algorithm

to predict cracks and their growth using the data collected from the curvature measurements. Although primarily done for silicon solar PV in this study, these ***CCAI*** approaches could be critical for stress and crack damage control for silicon semiconductor device/package reliability, especially with the ever-increasing trends of 3D stacking/integration and wafer-scale bonding (wafer-to-wafer bonding) requiring ultimate accuracy, manufacturing yield and product reliability.

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P48.PK

Crack Catcher AI – Enabling Smart Fracture Mechanics Approach for Damage Control in Thin Silicon Wafers for 3D Semiconductor Integrated Devices/Packages

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Introduction

Crack Catcher AI uses smart stress sensing and smart fracture sensing and prediction utilizing big data analytics to determine local stresses in the silicon solar cells which have led to propagation of cracks in the solar cells. This technology also applies to the semiconductor industry in wafer-to-wafer bonding process.

The poster outlines two key systems: **Smart Stress Sensing** (using laser technology) and **Smart Fracture Sensing and Prediction** (utilizing AI), both aimed at enhancing the efficiency and cost-effectiveness of next-generation silicon technologies (as shown in Fig. 1)

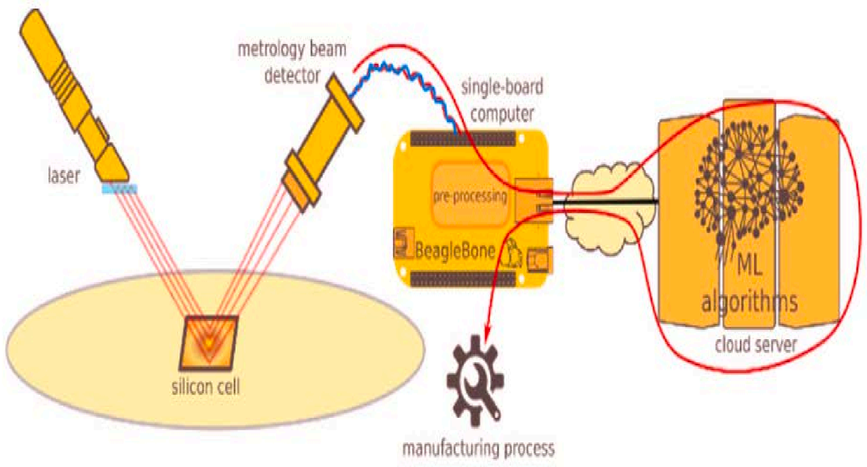

Fig. 1. Schematic illustration of optical (laser-based) inline metrology system and the data processing via BeagleBone and big data analysis by cloud computing machine algorithms.

Semiconductor Wafer Stress Mapping

Wafer-to-Wafer Bonding requires highly precise alignment between chips on one wafer to the chips on the other wafer it is to be bonded on, as illustrated in Fig. 2. Our proposed solution is ***Crack Catcher AI* – Smart Fracture Mechanics Approach in Thin Silicon Semiconductor Wafers for Enabling Wafer-to-Wafer Bonding in 3D Semiconductor Integrated Devices/Packages** which **uses** local stress metrology tool that would allow rapid mapping of local stresses in a silicon semiconductor wafer which enables use in high volume manufacturing or packaging assembly environments. With the local stress map in each wafer, each potential misalignment on every chip on the wafer may be mapped and optimization of alignment process of each wafer in the Wafer-to-Wafer Bonding process

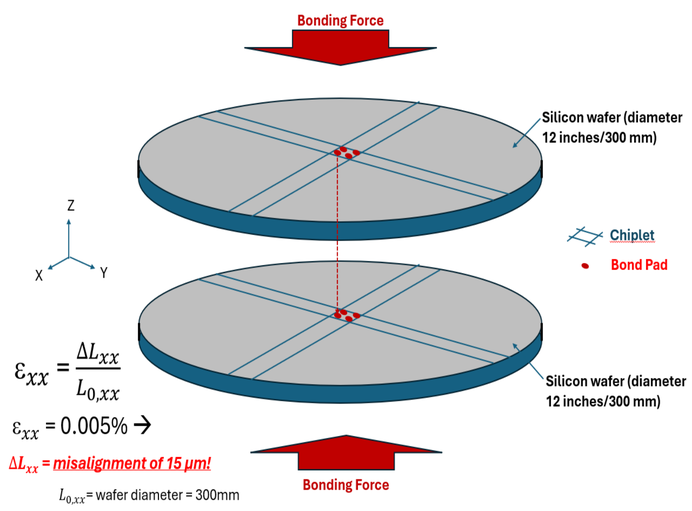

Fig. 2. Schematic illustration of Wafer-to-Wafer Bonding process and the key issue of misalignment due to local stresses in the large, thin silicon semiconductor wafers

Smart Stress Sensing

The **Smart Stress Sensing (SSS)** System is based on the high-resolution laser instrumentation and enabled by the local curvature technique. This technique is used to measure the local stress and map it as a function of position (X,Y) across the large silicon semiconductor wafer in high resolution (micron-scale), such as illustrated in Fig. 1.

The typical system measures wafer curvature by monitoring the deflection of parallel beams of laser (due to surface tilt or misorientation) and mapping would be enabled by high precision, servo motor controlled x-y stage as seen in Fig. 3.

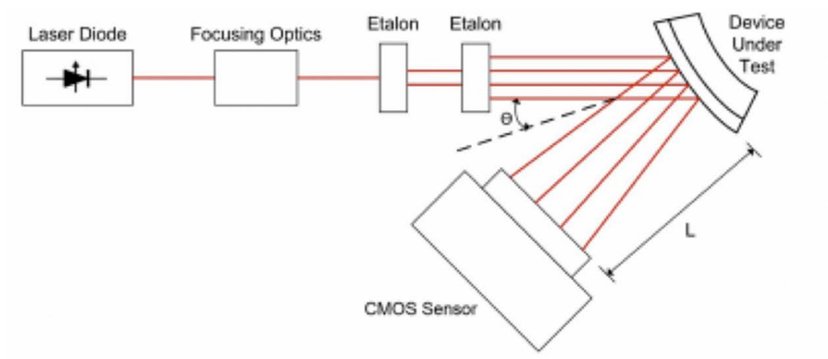

Fig. 3. Schematic of the fast waver curvature measurement using laser methodology.

Our latest **SSS** results are shown in Fig. 4, using the laser set up (not the synchrotron set up). Fig. 4(a) shows the experimental stress maps obtained from the laser measurement on areas around a metallization interconnect on the monocrystalline silicon cells. They show the high local stress concentration areas on the edges of the metal lines. Fig. 4(b) shows the simulation using FEA indicating good agreement to the experimental stress maps.

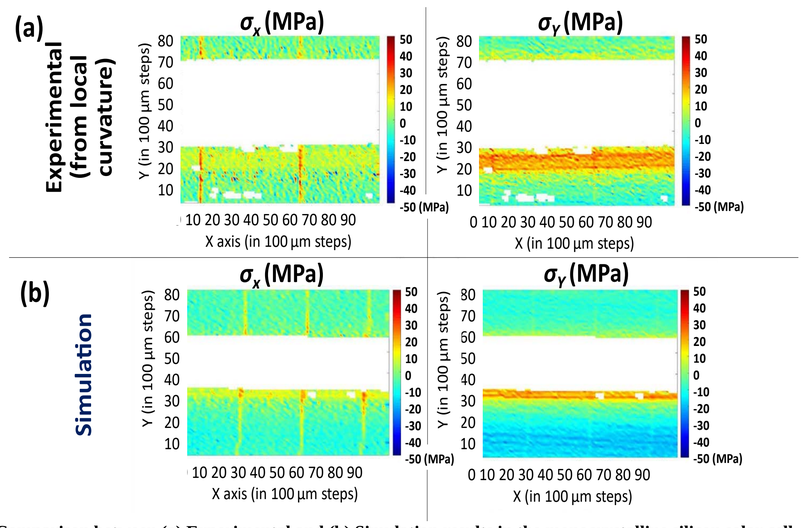

Fig.4. Comparison between (a) Experimental and (b) Simulation results in the monocrystalline silicon solar cell (unlaminated). The comparison suggests high degree of consistency in showing the high stress concentration areas (the stresses in X-direction (s_x) and Y-direction (s_y)).

Smart Fracture Sensing & Prediction

The Smart Fracture Sensing & Prediction (SFSP) System is based on **AI (Artificial Intelligence) and big data analytics.** This technique is used to detect and image defect/crack, map it as a function of position (X,Y) across the large silicon semiconductor wafer in high resolution (micron-scale) and predict the damage evolution or crack propagation based on AI and Machine Learning approaches, such as illustrated in Fig. 1.

The experiment results are shown in Figure 5. In these figures, the heuristic-based algorithm has marked all different crack lines and classify them by showing in different colour mark as different angle. The major angle are the ones shown in green which are the +/-45º. The other are different angles shown in blue and in orange which are happening in different frequencies (less frequent than the +/-45º).

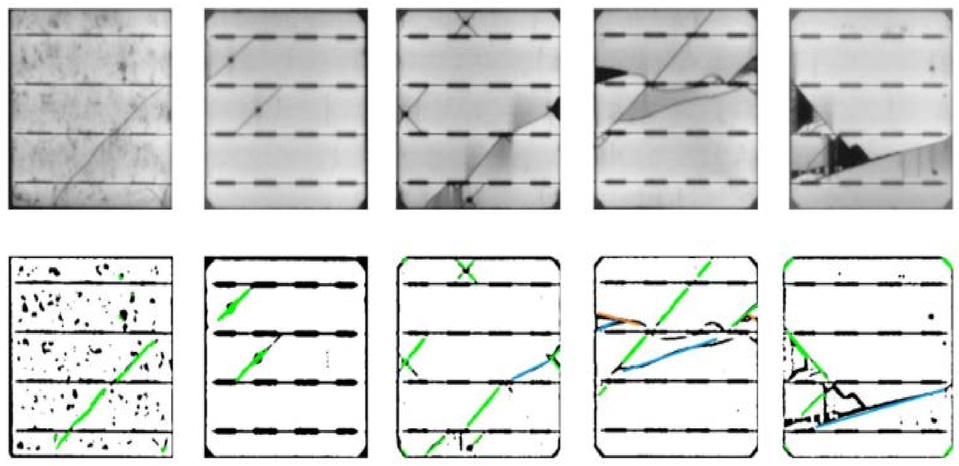

Fig. 5. Heuristic (Classic AI) experimental results.

Using a public dataset, the SFSP program indicates that 75.4% of all the crack lines belong to the angles (+/- 45°, +/- 6° and +/- 13°) that may be correlated with certain crystallographic planes of the single crystal silicon of the solar cell as shown in Table 1. This implies that crack propagates along certain preferred crystallographic planes at least 75.4% of the time, which has important role in crack prediction.

Angles Detected	Frequency / Count	Total Frequency Detected	Total Frequency	Occurrence (Detected) (%)	Overall Occurrence (%)
+/- 45°	166	278	310	59.7	53.5
+/- 6°	35	278	310	12.6	11.3
+/- 13°	33	278	310	11.9	10.6
+/- 20°	14	278	310	5.0	4.5
+/- 40°	8	278	310	2.9	2.6
+ 60°	8	278	310	2.9	2.6
+ 120°	7	278	310	2.5	2.3
+ 90	3	278	310	1.1	1.0
+ 110°	3	278	310	1.1	1.0
+ 70°	1	278	310	0.4	0.3
Undetected	32	NA	310	NA	10.3

Table 1 Crack Lines Detection Results using Object Detection based on YOLO v3 and ResNet 18 – Reordered By Rank

Conclusion

The Crack Catcher AI (CCAI) is a system that uses two key components. The first is a smart sensing technique that uses high resolution laser measurements to create a stress map of the silicon cell. The second component is an AI algorithm to predict cracks and their growth using the data collected from the curvature measurements. Although primarily done for silicon solar PV in this study, these CCAI approaches could be critical for stress and damage control for silicon semiconductor device/package reliability, especially with the ever-increasing trends of 3D stacking/integration and wafer-scale bonding (wafer-to-wafer bonding) requiring ultimate accuracy, manufacturing yield and product reliability.

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ABSTRACT

The importance of silicon cannot be undermined – in photovoltaics (PV) as well as in semiconductor industries. However, silicon is very brittle. Silicon cells/wafers crack easily during manufacturing assembly and/or during device operations. *Crack Catcher AI* uses novel smart fracture mechanics approach with Artificial Intelligence (AI) methodologies to predict and control crack/damage evolution in thin silicon cells/wafers. This is critical as semiconductor 3D integration technology calls for wafer-to-wafer bonding with utmost alignment accuracy and yield/reliability.

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Gabriel Preston is a student at Oregon Institute of Technology studying mechanical and manufacturing engineering and a Research Assistant at OREC (Oregon Renewable Energy Center). He has been on the research team at Crack Catcher AI (CCAI) under Prof. Arief Budiman's leadership since March of 2023 where he helps perform tests and stress calculations and analyses. He enjoys the hands on experience that this project and OIT has provided as a research student and research assistant in OREC. Gabriel is looking forward to a career that challenges his knowledge on materials, design and stress analysis.

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